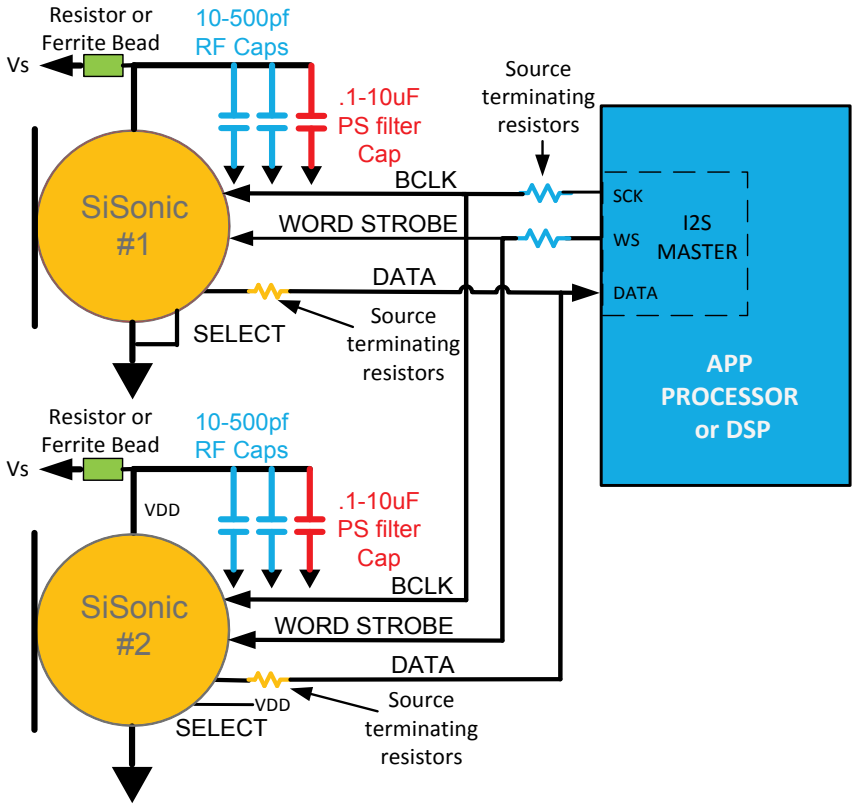
I2S Digital Microphone Test

Introduction

Other than the traditional Pulse Density Modulation digital microphone, SPH0645LM4H-B is the first miniature, high-performance, low power, bottom port silicon digital microphone that support standard I2S interface in Knowles microphone families. Using Knowles' proven high performance SiSonic™ MEMS technology, SPH0645LM4H-B consists of an acoustic sensor, a low noise input buffer, a serial analog to digital convertor. It allows direct connection between microphone and application processor or DSP. This device is suitable for portable electronic devices where voice control, wideband audio performance, RF immunity and low current are required.

Reference Application Circuit



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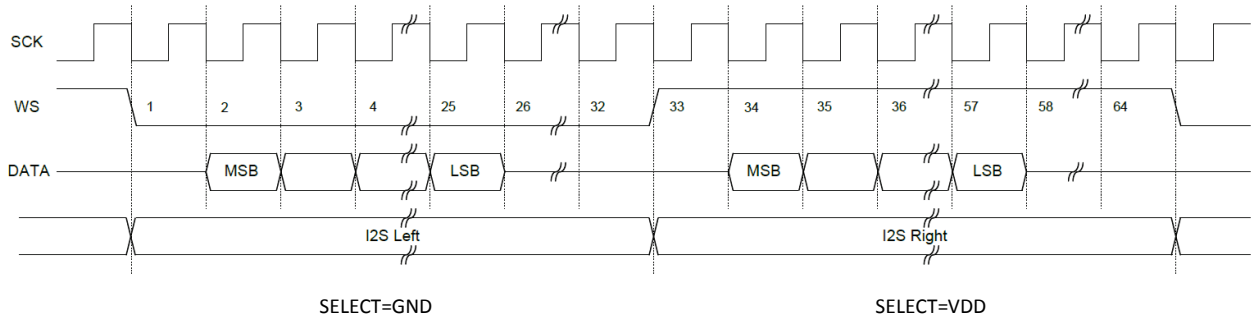
I2S Digital Microphone Interface

A typical I2S interface provides a SCK and a WS signal. SCK is used in the ADC as well as to serialize the bits. WS is used to define the data framing and has a frequency which is 64 times slower than the BCK frequency and with a 50% duty cycle to allow the two microphones a 32 bit time slot each. Depending on the voltage level on SELECT, the microphone provides the DATA output either during the left channel frame or during the right channel frame. The Data word length from the microphone is 24 bits, it contains an 18 bits filtered data and the LSRs are filled up with zeroes. The microphone samples will be synchronized on the falling edge of the word strobe signal to allow acoustic signal processing on the input signal of both microphones simultaneously. If more than two microphones are needed, the word strobe of all microphones used in the system should be synchronized to assure that all microphones are sampled at the same physical time.



I2S Clock Timing Diagram

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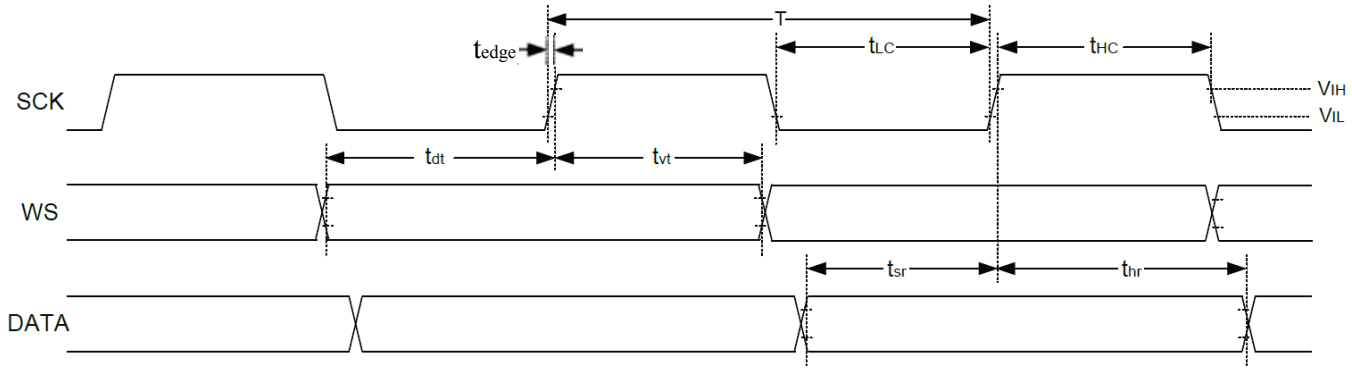
I2S Digital Microphone Timing Requirements

Parameter	Symbol	Min	Max	Unit	Note
Clock Period of SCK	T	244.14	488.28	ns	
Clock Edge Time	t_{edge}		3.75	ns	Measured between 0.35*VDD and 0.65*VDD, typical operation conditions (1) (2)
High Time	t_{HC}	97.8	293.1	ns	
Low Time	t_{LC}	97.8	293.1	ns	
Delay Time	t_{dt}	48.9		ns	
Valid Time	t_{vt}	0		ns	
Setup Time	t_{sr}	195.3		ns	
Hold Time	t_{hr}	0		ns	
Logic Input High	V_{IH}	VDD-0.2V	3.6	V	
Logic Input Low	V_{IL}	GND	GND+0.2V	V	

Note:
(1) If the DATA line is shared between two microphones, the required clock edge might be faster to guarantee non-overlapping phases.
(2) Corresponds to 10ns between 10% and 90% of VDD. Slower clock edges are possible, but noise on CLK and supply lines might affect performance.



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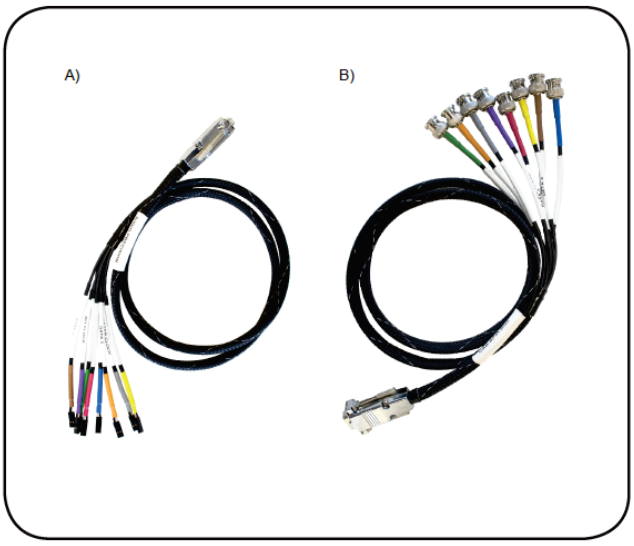
I2S Digital Microphone Test With APx 525

Apx525 family from Audio Precision is an excellent choice for R&D engineers and production technicians who want fast and easy analog and digital audio test.

With APx Digital Serial I/O Option and CAB-DSIO cable kit, user can analyze the I2S digital signal directly from SPH0645LM4H-B without spending resource of design a I2S to analog convertor or subtract the effect of the DAC from the end result.

CAB-DSIO Cable Kit

for APx Series audio analyzers



Contents

A) 1 each DB15M to 8 2-pin breakout cable
B) 1 each DB15M to 8 BNC breakout cable

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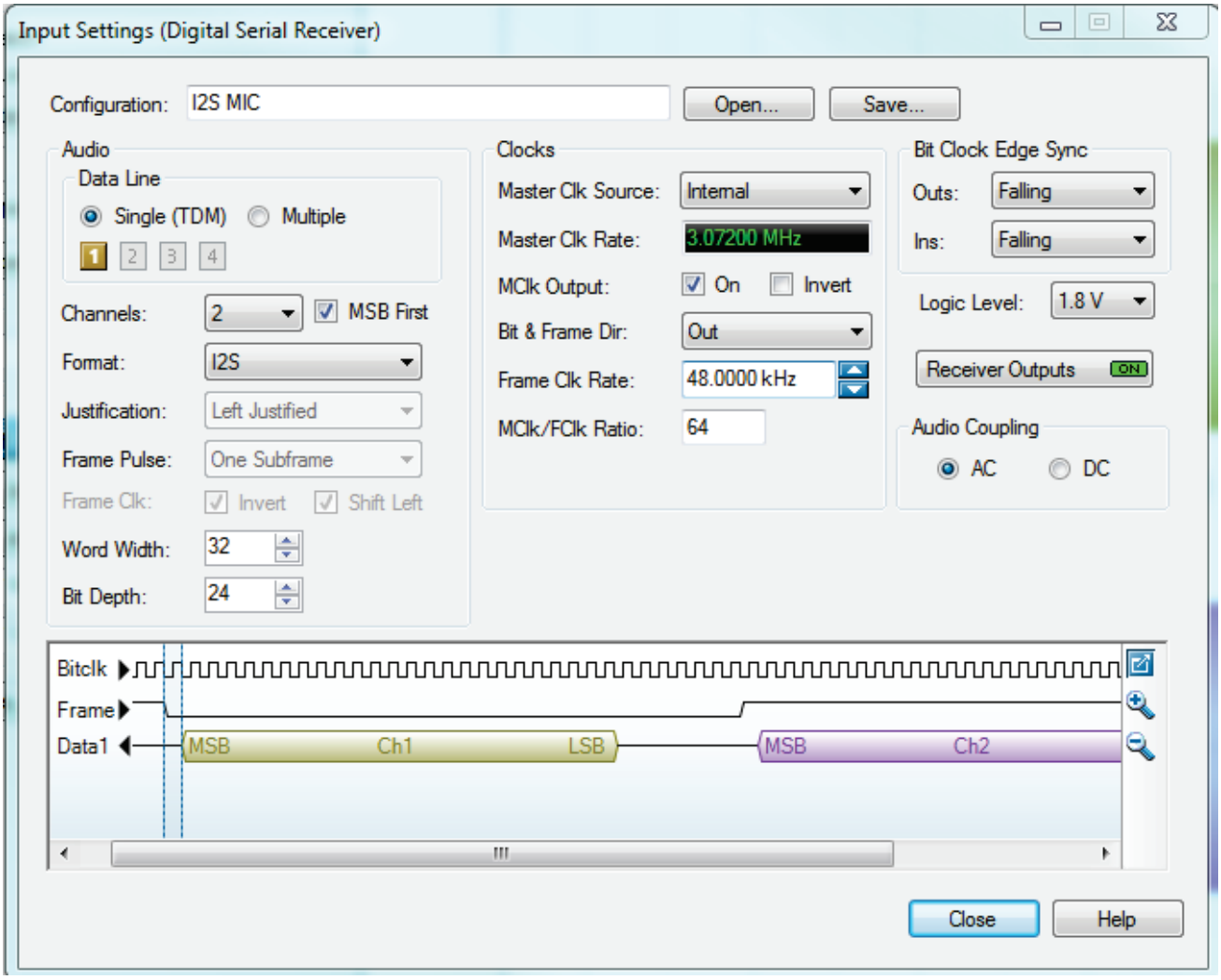
Here's an example of SPH0645LM4H-B test with APx525:



APx525 Software Setting

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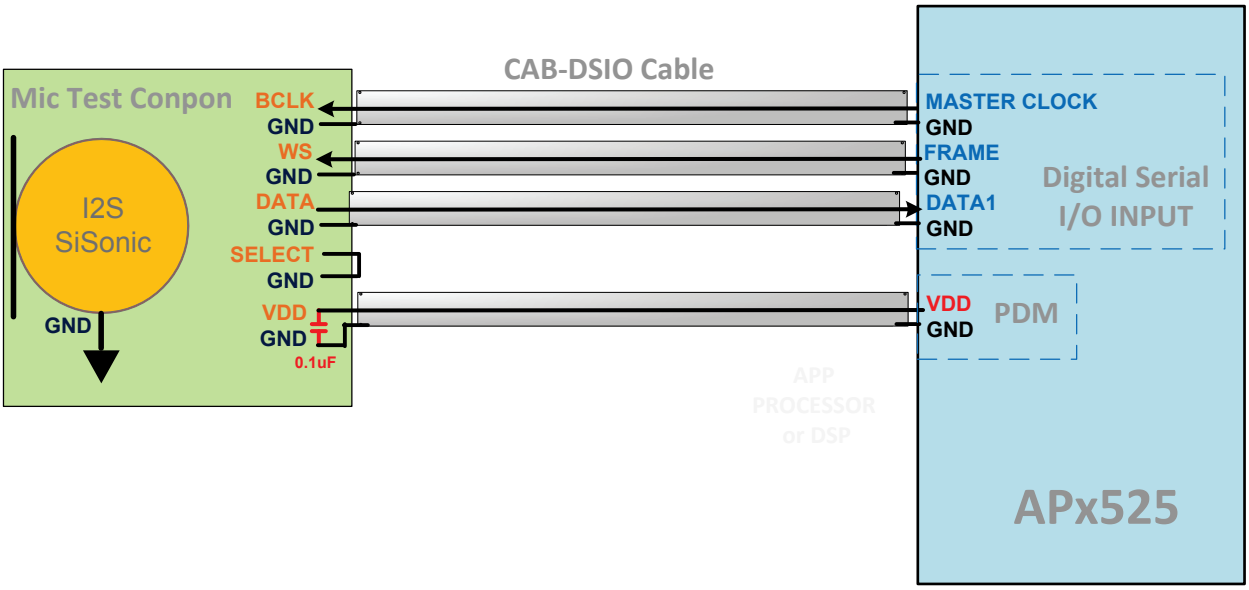

Test Diagram

Importance Test Notes:

- ✓ A 0.1~10uF power supply decoupling cap closed to DUT is needed to reduce noise coupling (this is a comment rule for digital system).
- ✓ The provided clock is also used for sampling the input signal, the clock frequency has to be stable, continuously running and must have low jitter.
- ✓ SPH0645LM4H-B is not design to drive long cable (>4 feet). Short (<2 feet) and low capacitance (<30pF/ft) 50 ohm high quality coax cable (such as AP's test cable or Mil type RG cable) is recommended. Loading microphone with long cables will greatly degrade microphone's performance or fail to detect microphone signal in some severe cases.

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